REMARKS

In view of the preceding amendments and the comments which follow, and pursuant to 37 C.F.R. § 1.111, amendment and reconsideration of the Official Action of December 22, 2004 is respectfully requested by Applicant.

Summary

Claims 1 – 4 stand rejected. Claims 1 and 3 have been amended. No new matter has been introduced as a result of this amendment. Claims 1 – 4 are pending following entry of the present remarks.

Claim Rejections under 35 USC §102

The Examiner has rejected Claims 1 and 2 under U.S.C. 102(e) as being anticipated by Delano (U.S. Patent No.: 6,577,194 B2).

Claim 1 is directed to an amplifying circuit for a transmitter. The amplifying circuit has a first switching device connected to a power supply, a second switching device connected to the first switching device at one end and grounded at another end, and a load connected to a junction point of the first switching device and the second switching device.

The first and second switching devices are driven by a driving circuit. This driving circuit has an inverting circuit connected to a control electrode of the second switching device. Delano does not anticipate or disclose such a driving circuit. For example, Delano does not anticipate or disclose an inverting circuit that is connected to a control electrode of the second switching device.

Moreover, Claim 1 recites that the input signals are provided invertedly to the second switching device with respect to the first switching device, that is, the input signals are applied "in-phase" to the first and second switching devices. Delano does not anticipate or disclose that the input signal to control electrode of the second switching device is inverted with respect to the input signal of the first switching device. In fact, Delano states that the top and bottom side FETs (102) and (104) are alternately driven by gating signals which are generated from the output of A/D converter (106) by gate driven circuitry (108) (See Figure 1 and Column 1, lines 27 – 29). In contrast to the

arrangement of Claim 1 in which the signals are applied in-phase, in Delano the input signals to the FETs (102) and (104) are applied alternately.

Accordingly, Claim 1 is not anticipated by Delano. Thus, Claim 1 is allowable. Dependent Claim 2 is allowable for at least the same reasons.

The Examiner has rejected Claims 3 and 4 under U.S.C. 102(b) as being anticipated by Andreatta (U.S. Patent No.: 3,239,771). Claim 3 has been amended.

As amended, Claim 3 now recites that an input signal inverted with respect to an input signal of the first switching device is applied to the control electrode of the second switching device. Thus, the input signals are provided invertedly to the first and second switching devices.

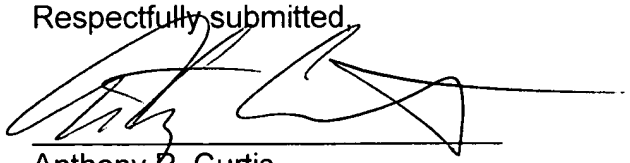
Similar to the above discussion with respect to Delano, Andreatta fails to anticipate or disclose an inverter circuit (let alone multiple inverter circuits) in the driving circuit as well as failing to anticipate or disclose specifics about the input signals between the first and second switching devices being inverted, as well as the input signals between the third and fourth switching devices being inverted.

Accordingly, Claim 3 is not anticipated by Andreatta. Thus, Claim 3 is allowable. Dependent Claim 4 is allowable for at least the same reasons.

CONCLUSION

Pending Claims 1 - 4 are patentable. Applicant respectfully requests the Examiner grant allowance of this application. The Examiner is invited to contact the undersigned attorney for the Applicant via telephone if such communication would expedite this application.

Respectfully submitted,



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